Appendix D
Class Codes

9908.05

This appendix describes the current Class Code encodings. This list may be enhanced at any time. The PCI SIG web pages contain

Base Class	Meaning
00h	Device was built before Class Code definitions were finalized.
01h	Mass storage controller.
02h	Network controller.
03h	Display controller.
04h	Multimedia device.
05h	Memory controller.
06h	Bridge device.
07h	Simple communication controllers.
08h	Base system peripherals.
09h	Input devices.
0Ah	Docking stations.
0Bh	Processors.
0Ch	Serial bus controllers.
0Dh	Wireless controllers.
0Eh	Intelligent IO Controllers.
0Fh	Satellite communication controllers.
10h	Encryption/Decryption controllers.
11h	Data acquisition and signal processing controllers.
12h - FEh	Reserved.
FFh	Device does not fit in any defined classes.

the latest version. Companies wishing to define a new encoding should contact the PCI SIG. All unspecified values are reserved for SIG assignment.

Base Class 00h

This base class is defined to provide backward compatibility for devices that were built before the Class Code field was defined. No new devices should use this value and existing devices should switch to a more appropriate value if possible.
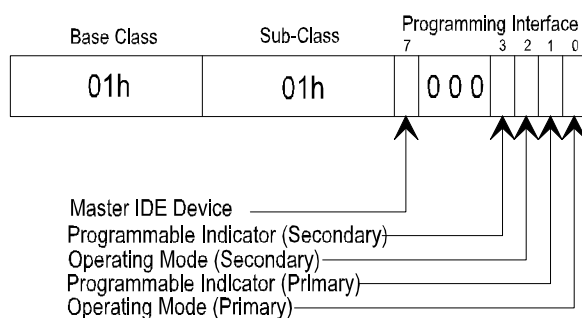
For class codes with this base class value, there are two defined values for the remaining fields as shown in the table below. All other values are reserved.

Base Class	Sub-Class	Interface	Meaning
00h	00h	00h	All currently implemented devices except VGA-compatible devices.
	01h	00h	VGA-compatible device.

Base Class 01h

This base class is defined for all types of mass storage controllers. Several sub-class values are defined. The IDE controller class is the only one that has a specific register-level programming interface defined.

Base Class	Sub-Class	Interface	Meaning
01h	00h	00h	SCSI bus controller.
	01h	xxh	IDE controller (see below).
	02h	00h	Floppy disk controller.
	03h	00h	IPI bus controller.
	04h	00h	RAID controller.
	80h	00h	Other mass storage controller.

Figure D-1: Programming Interface Byte Layout for IDE Controller Class Code

The SIG document *PCI IDE Controller Specification* completely describes the layout and meaning of bits 0 thru 3 in the Programming Interface byte. The document *Bus Master Programming Interface for IDE ATA Controllers* describes the meaning of bit 7 in the Programming Interface byte. This document can be obtained via FAX by calling (408)741-1600 and requesting document 8038.

Base Class 02h

This base class is defined for all types of network controllers. Several sub-class values are defined. There are no register-level programming interfaces defined.

Base Class	Sub-Class	Interface	Meaning
02h	00h	00h	Ethernet controller.
	01h	00h	Token Ring controller.
	02h	00h	FDDI controller.
	03h	00h	ATM controller.
	04h	00h	ISDN controller
	80h	00h	Other network controller.

Base Class 03h

This base class is defined for all types of display controllers. For VGA devices (Sub-Class 00h), the programming interface byte is divided into a bit field that identifies additional video controller compatibilities. A device can support multiple interfaces by using the bit map to indicate which interfaces are supported. For the XGA devices (Sub-Class 01h), only the standard XGA interface is defined. Sub-Class 02h is for controllers that have hardware support for 3D operations and are not VGA compatible.

Base Class	Sub-Class	Interface	Meaning
03h	00h	00000000b	VGA-compatible controller. Memory addresses 0A0000h thru 0BFFFFh. I/O addresses 3B0h to 3BBh and 3C0h to 3DFh and all aliases of these addresses.
		00000001b	8514-compatible controller -- 2E8h and its aliases, 2EAh-2EFh.
	01h	00h	XGA controller.
	02h	00h	3D controller
	80h	00h	Other display controller.

Base Class 04h

This base class is defined for all types of multimedia devices. Several sub-class values are defined. There are no register-level programming interfaces defined.

Base Class	Sub-Class	Interface	Meaning
04h	00h	00h	Video device.
	01h	00h	Audio device.
	02h	00h	Computer telephony device.
	80h	00h	Other multimedia device.

Base Class 05h

This base class is defined for all types of memory controllers (refer to Section 6.2.5.3). Several sub-class values are defined. There are no register-level programming interfaces defined.

Base Class	Sub-Class	Interface	Meaning
05h	00h	00h	RAM.
	01h	00h	Flash.
	80h	00h	Other memory controller.

Base Class 06h

This base class is defined for all types of bridge devices. A PCI bridge is any PCI device that maps PCI resources (memory or I/O) from one side of the device to the other. Several sub-class values are defined.

Base Class	Sub-Class	Interface	Meaning
06h	00h	00h	Host bridge.
	01h	00h	ISA bridge.
	02h	00h	EISA bridge.
	03h	00h	MCA bridge.
	04h	00h	PCI-to-PCI bridge.
		01h	Subtractive Decode PCI-to-PCI Bridge. This interface code identifies the PCI-to-PCI bridge as a device that supports subtractive decoding in addition to all the currently defined functions of a PCI-to-PCI bridge.
	05h	00h	PCMCIA bridge.
	06h	00h	NuBus bridge.
	07h	00h	CardBus bridge.
	08h	xxh	RACEway bridge. (see below)
	09h	40h	Semi-transparent PCI-to-PCI bridge with the Primary PCI Bus side facing the system Host processor.
		80h	Semi-transparent PCI-to-PCI bridge with the Secondary PCI Bus side facing the system Host processor.
	80h	00h	Other bridge device.

RACEway is an ANSI standard (ANSI/VITA 5-1994) switching fabric. For the Programming Interface bits, [7:1] are reserved, read-only and return zeros. Bit 0 defines the operation mode and is read-only:

> 0 - Transparent mode

> 1 - End-point mode

Base Class 07h

This base class is defined for all types of simple communications controllers. Several sub-class values are defined, some of these having specific well-known register-level programming interfaces.

Base Class	Sub-Class	Interface	Meaning
07h	00h	00h	Generic XT-compatible serial controller.
		01h	16450-compatible serial controller.
		02h	16550-compatible serial controller.
		03h	16650-compatible serial controller.
		04h	16750-compatible serial controller.
		05h	16850-compatible serial controller.
		06h	16950-compatible serial controller.
	01h	00h	Parallel port.
		01h	Bidirectional parallel port.
		02h	ECP 1.X compliant parallel port.
		03h	IEEE1284 controller
		FEh	IEEE1284 target device (not a controller)
	02h	00h	Multiport Serial Controller
	03h	00h	Generic Modem
		01h	Hayes compatible modem, 16450-compatible interface (see below)
		02h	Hayes compatible modem, 16550-compatible interface (see below)
		03h	Hayes compatible modem, 16650-compatible interface (see below)
		04h	Hayes compatible modem, 16750-compatible interface (see below)
	80h	00h	Other communications device.

For Hayes-compatible modems, the first base address register (at offset 10h) maps the appropriate compatible (i.e. 16450, 16550, etc.) register set for the serial controller at the beginning of the mapped space. Note that these registers can be either memory or IO mapped depending what kind of BAR is used.

Base Class 08h

This base class is defined for all types of generic system peripherals. Several sub-class values are defined, most of these having a specific well-known register-level programming interface.

Base Class	Sub-Class	Interface	Meaning
08h	00h	00h	Generic 8259 PIC.
		01h	ISA PIC.
		02h	EISA PIC.
		10h	I/O APIC Interrupt Controller (see below)
	01h	00h	Generic 8237 DMA controller.
		01h	ISA DMA controller.
		02h	EISA DMA controller.
	02h	00h	Generic 8254 system timer
		01h	ISA system timer.
		02h	EISA system timers (two timers).

	03h	00h	Generic RTC controller.
		01h	ISA RTC controller.
	04h	00h	Generic PCI Hot-Plug controller
	80h	00h	Other system peripheral.

For I/O APIC Interrupt Controller, the Base Address Register at offset 0x10 is used to request a minimum of 32 bytes of non-prefetchable memory. Two registers within that space are located at Base+0x00 (I/O Select Register) and Base+0x10 (I/O Window Register). For a full description of the use of these registers please refer to the data sheet for the Intel 8237EB in the 82420/82430 PCIset EISA Bridge Databook #290483-003.

Base Class 09h

This base class is defined for all types of input devices. Several sub-class values are defined. A register-level programming interface is defined for Gameport controllers.

Base Class	Sub-Class	Interface	Meaning
09h	00h	00h	Keyboard controller.
	01h	00h	Digitizer (pen).
	02h	00h	Mouse controller.
	03h	00h	Scanner Controller.
	04h	00h	Gameport Controller (generic)
		10h	Gameport Controller (see below)
	80h	00h	Other input controller.

A Gameport controller with a Programming Interface == 10h indicates that any Base Address registers in this function that request/assign IO address space, the registers in that IO space conform to the standard 'legacy' game ports. The byte at offset 00h in an IO region behaves as a legacy gameport interface where reads to the byte return joystick/gamepad information, and writes to the byte start the RC timer. The byte at offset 01h is an alias of the byte at offset 00h. All other bytes in an IO region are unspecified and can be used in vendor unique ways.

Base Class 0Ah

This base class is defined for all types of docking stations. No specific register-level programming interfaces are defined.

Base Class	Sub-Class	Interface	Meaning
0Ah	00h	00h	Generic docking station.
	80h	00h	Other type of docking station.

Base Class 0Bh

This base class is defined for all types of processors. Several sub-class values are defined corresponding to different processor types or instruction sets. There are no specific register-level programming interfaces defined.

Base Class	Sub-Class	Interface	Meaning
0Bh	00h	00h	386.
	01h	00h	486.
	02h	00h	Pentium.
	10h	00h	Alpha.
	20h	00h	PowerPC.
	30h	00h	MIPS
	40h	00h	Co-processor.

Base Class 0Ch

This base class is defined for all types of serial bus controllers. Several sub-class values are defined. There are specific register-level programming interfaces defined for Universal Serial Bus Controllers and IEEE 1394 Controllers.

Base Class	Sub-Class	Interface	Meaning
0Ch	00	00h	IEEE 1394 (FireWire).
		10h	IEEE 1394 following the 1394 OpenHCI specification
	01h	00h	ACCESS.bus.
	02h	00h	SSA.
	03h	00h	Universal Serial Bus (USB) following the Universal Host Controller Specification.
		10h	Universal Serial Bus (USB) following the Open Host Controller Specification.
		80h	Universal Serial Bus with no specific programming interface
		FEh	USB device (not host controller)
	04h	00h	Fibre Channel.
	05h	00h	SMBus (System Management Bus)

Base Class 0Dh

This base class is defined for all types of wireless controllers. Several sub-class values are defined. There are no specific register-level programming interfaces defined.

Base Class	Sub-Class	Interface	Meaning
0Dh	00	00h	iRDA compatible controller
	01h	00h	Consumer IR controller
	10h	00h	RF Controller
	80h	00h	Other type of Wireless controller

Base Class 0Eh

This base class is defined for intelligent IO controllers. The primary characteristic of this base class is that the IO function provided follows some sort of generic definition for an IO controller.

Base Class	Sub-Class	Interface	Meaning
0Eh	00	xxh	Intelligent I/O (I2O) Architecture Specification 1.0
		00h	Message FIFO at offset 040h

The Specification for Intelligent I/O Architecture I/O can be downloaded from:

ftp.intel.com/pub/IAL/i2o/

Base Class 0Fh

This base class is defined for satellite communication controllers. Controllers of this type are used to communicate with satellites.

Base Class	Sub-Class	Interface	Meaning
0Fh	01h	00h	TV
	02h	00h	Audio
	03h	00h	Voice
	04h	00h	Data

Base Class 10h

This base class is defined for all types of encryption and decryption controllers. Several sub-class values are defined. There are no register-level interfaces defined.

Base Class	Sub-Class	Interface	Meaning
10h	00h	00h	Network & Computing En/Decryption
	10h	00h	Entertainment En/Decryption
	80h	00h	Other En/Decryption

Base Class 11h

This base class is defined for all types of data acquisition and signal processing controllers. Several sub-class values are defined. There are no register-level interfaces defined.

Base Class	Sub-Class	Interface	Meaning
11h	00h	00h	DPIO modules
	80h	00h	Other data acquisition/signal processing controllers